IN THE CLAIMS

Please amend the Claims as follows:

1. (previously presented) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing an organic dielectric layer overlying said insulating layer;

depositing an inorganic dielectric layer overlying said organic dielectric layer wherein no etch stop layer is formed between said organic dielectric layer and said inorganic dielectric layer;

etching a via pattern into said inorganic dielectric layer;

etching said via pattern into said organic dielectric layer using patterned said inorganic dielectric layer as a mask; and

thereafter etching a trench pattern into said inorganic dielectric layer wherein said organic dielectric layer acts as an etch stop to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

2. (original) The method according to Claim 1 further comprising forming semiconductor device structures including gate electrodes and source and drain regions in and on said semiconductor substrate wherein said metal lines overlie and contact said semiconductor device structures.

3. (previously presented) The method according to Claim 1 wherein said organic dielectric layer comprises polyimides, HOSP, SILK, FLARE, benzocyclobutene (BCB), methylsilsesquioxane (MSQ), or organic polymers.

4. (previously presented) The method according to Claim 1 wherein said inorganic dielectric layer comprises CORAL, BLACK DIAMOND, fluorinated silicate glass (FSG), carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, or hydrogen silsesquioxane (HSQ).

5. (original) The method according to Claim 1 further comprising filling said dual damascene openings with a metal layer.

6. (previously presented) A method of forming dual damascene openings in the fabrication of an integrated

circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing an organic dielectric layer overlying said insulating layer;

depositing an inorganic dielectric layer overlying said organic dielectric layer wherein no etch stop layer is formed between said organic dielectric layer and said inorganic dielectric layer;

etching a trench pattern into said inorganic dielectric layer; and

thereafter etching a via pattern into said organic dielectric layer through said trench pattern to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

7. (original) The method according to Claim 6 further comprising forming semiconductor device structures including gate electrodes and source and drain regions in and on said semiconductor substrate wherein said metal lines overlie and contact said semiconductor device structures.

8. (previously presented) The method according to Claim 6 wherein said organic dielectric layer comprises

polyimides, HOSP, SILK, FLARE, benzocyclobutene (BCB), methylsilsesquioxane (MSQ), or organic polymers.

9. (previously presented) The method according to Claim 6 wherein said inorganic dielectric layer comprises CORAL, BLACK DIAMOND, fluorinated silicate glass (FSG), carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, or hydrogen silsesquioxane (HSQ).

10. (original) The method according to Claim 6 further comprising filling said dual damascene openings with a metal layer.

11. (currently amended) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing an organic dielectric layer overlying said insulating layer;

depositing an inorganic dielectric layer overlying said organic dielectric layer wherein no etch stop layer is formed between said organic dielectric layer and said inorganic dielectric layer;

etching a via pattern into said inorganic

dielectric layer; and

thereafter simultaneously etching said via pattern into said organic dielectric layer and etching a trench pattern into said inorganic dielectric layer wherein one etching recipe is used for said organic dielectric layer and a different etching recipe is used for said inorganic dielectric layer to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

12. (original) The method according to Claim 11 further comprising forming semiconductor device structures including gate electrodes and source and drain regions in and on said semiconductor substrate wherein said metal lines overlie and contact said semiconductor device structures.

13. (previously presented) The method according to Claim 11 wherein said organic dielectric layer comprises polyimides, HOSP, SILK, FLARE, benzocyclobutene (BCB), methylsilsesquioxane (MSQ), or organic polymers.

14. (previously presented) The method according to Claim 11 wherein said inorganic dielectric layer comprises CORAL, BLACK DIAMOND, fluorinated silicate glass (FSG),

carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, or hydrogen silsesquioxane (HSQ).

15. (original) The method according to Claim 11 further comprising filling said dual damascene openings with a metal layer.

16. (previously presented) A method of forming dual damascene openings in the fabrication of an integrated circuit device comprising:

providing metal lines covered by an insulating layer overlying a semiconductor substrate;

depositing an inorganic dielectric layer overlying said insulating layer;

depositing an organic dielectric layer overlying said inorganic dielectric layer wherein no etch stop layer is formed between said inorganic dielectric layer and said organic dielectric layer;

etching a via pattern into said organic dielectric layer;

etching said via pattern into said inorganic dielectric layer using patterned said organic dielectric layer as a mask; and

thereafter etching a trench pattern into said organic dielectric layer wherein said inorganic

dielectric layer acts as an etch stop to complete said forming of said dual damascene openings in the fabrication of said integrated circuit device.

17. (original) The method according to Claim 16 further comprising forming semiconductor device structures including gate electrodes and source and drain regions in and on said semiconductor substrate wherein said metal lines overlie and contact said semiconductor device structures.

18. (previously presented) The method according to Claim 16 wherein said inorganic dielectric layer comprises CORAL, BLACK DIAMOND, fluorinated silicate glass (FSG), carbon-doped FSG, nitrogen-doped FSG, Z3MS, XLK, or hydrogen silsesquioxane (HSQ).

19. (previously presented) The method according to Claim 16 wherein said organic dielectric layer comprises polyimides, HOSP, SILK, FLARE, benzocyclobutene (BCB), methylsilsesquioxane (MSQ), or organic polymers.

20. (original) The method according to Claim 16 further comprising filling said dual damascene openings with a metal layer.

21-30. (canceled)